CLAIMS

What is claimed is:

1. A method for making a resistive heater for a planar lightwave circuit, the method comprising the steps of:

a) depositing a resistive layer on a top clad of a planar lightwave circuit;

b) depositing an interconnect layer over the resistive layer;

c) etching the interconnect layer to define a heater interconnect, wherein the heater interconnect is disposed over the resistive layer and has a first width;

d) masking the heater interconnect; and

e) etching the resistive layer to define a resistive heater, wherein the resistive heater is disposed beneath the heater interconnect and has a second width larger than the first width.

2. The method of claim 1 wherein the heater interconnect is defined to include a heater conduct region between a first contact pad and a second contact pad such that a current between the first contact pad and the second contact pad is conducted through the resistive heater.

3. The method of claim 1 wherein the resistive layer comprises tungsten and the interconnect layer comprises aluminum.

4. The method of claim 1 wherein the difference between the first width of the heater interconnect and the second width of the resistive heater is determined to decrease an alignment sensitivity of a lithography process for masking the heater interconnect.

5. The method of claim 1 further including the step of using a dry etch process to etch the interconnect layer.

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6. The method of claim 5 wherein the dry etch process is a reactive ion etching process.

7. The method of claim 1 further including the step of using a dry etch process to etch the resistive layer.

8. The method of claim 7 wherein the dry etch process is a reactive ion etching process.

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9. A method for making a resistive heater for an active planar lightwave circuit, the method comprising the steps of:

a) depositing a tungsten resistive layer on a top clad of a planar lightwave circuit;

b) depositing an aluminum interconnect layer over the resistive layer such that the tungsten resistive layer functions as an adhesion layer for the aluminum interconnect layer;

c) etching the aluminum interconnect layer to define a heater interconnect, wherein the heater interconnect is disposed over the tungsten resistive layer and has a first width;

d) masking the heater interconnect; and

e) etching the tungsten resistive layer to define a resistive heater, wherein the resistive heater is disposed beneath the heater interconnect and has a second width larger than the first width.

10. The method of claim 9 wherein the heater interconnect is defined to include a heater conduct region between a first contact pad and a second contact pad such that a current between the first contact pad and the second contact pad is conducted through the resistive heater.

11. The method of claim 9 further including the step of using a wet etch process to etch the aluminum interconnect layer, wherein the wet etch process does not attack the tungsten resistive layer.

12. The method of claim 9 wherein the difference between the first width of the heater Interconnect and the second width of the resistive heater is determined to decrease an alignment sensitivity of a lithography process for masking the heater interconnect.

13. The method of claim 9 further including the step of using a dry etch process to etch the interconnect layer.

14. The method of claim 13 wherein the dry etch process is a reactive ion etching process.

15. The method of claim 9 further including the step of using a dry etch process to etch the resistive layer.

16. The method of claim 15 wherein the dry etch process is a reactive ion etching process.

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17. A method for making a thermo-optic resistive heater for an active planar lightwave circuit, the method comprising the steps of:

a) depositing a tungsten layer on a top clad of a planar lightwave circuit;

b) depositing an aluminum layer over the tungsten layer such that the tungsten layer functions as an adhesion layer for the aluminum layer;

c) masking a region of the aluminum layer to be subsequently defined as a heater interconnect;

d) etching the aluminum layer to define the heater interconnect, wherein the heater interconnect is disposed over the tungsten layer and has a first width;

e) masking the heater interconnect and masking a region of the tungsten layer to be subsequently defined as a resistive heater; and

f) etching the tungsten resistive layer to define the resistive heater, wherein the resistive heater is disposed beneath the heater interconnect and has a second width larger than the first width.

18. The method of claim 17 wherein the heater interconnect is defined to include a heater conduct region between a first contact pad and a second contact pad such that a current between the first contact pad and the second contact pad is conducted through the resistive heater.

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19 The method of claim 17 further including the step of using a wet etch process to etch the aluminum interconnect layer, wherein the wet etch process does not attack the tungsten resistive layer.

20. The method of claim 17 wherein the difference between the first width of the heater interconnect and the second width of the resistive heater is

determined to decrease an alignment sensitivity of a lithography process for masking the heater interconnect.

21. The method of claim 1 wherein the resistive layer is a refractory metal or an alloy of a refractory metal.

22. The method of claim 1 wherein the resistive layer includes titanium, cobalt, or nickel, and the interconnect layer includes aluminum, gold, or copper.